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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,142	11/16/2001	James S. Dunn	BUR920000140US1	4751

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EXAMINER

LEE, EUGENE

ART UNIT PAPER NUMBER

2815

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/991,142

Applicant(s)

DUNN ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-14 and 20-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-14 and 20-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference character "168" (see page 7, second paragraph). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 thru 3, 5, 7 thru 9, 12, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Khajezadeh 4,202,006. Khajezadeh discloses (see, for example, Fig. 1) a substrate 14, island (first semiconductor device) 28, island (second semiconductor device) 26, first buried pocket (first subcollector) 22, and second buried pocket (second subcollector) 20. In column 2, lines 16-17, Khajezadeh discloses the first buried pocket comprising antimony and the second buried pocket comprising arsenic. Regarding claim 5, by virtue of the second buried pocket being doped with arsenic and the first buried pocket being doped with antimony, the second buried pocket has a higher resistance and a higher breakdown voltage than the first buried pocket. Regarding claims 8 and 9, see, for example, region 46.

4. Claims 1 thru 5, 7 thru 9, 12, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohkawa et al. 5,798,560. Ohkawa discloses (see, for example, FIG. 3) a bipolar semiconductor integrated circuit comprising a substrate (wafer) 25, first transistor 22 and second transistor 23 wherein first transistor 22 comprises a buried N+ layer (first subcollector) 26 and second transistor 23 comprises a buried N+ layer (second subcollector) 26. In column 6, lines 6-8, Ohkawa discloses the buried N+ layer comprising antimony or arsenic. Regarding claims 8 and 9, see P+ region 27a.

5. Claims 1 thru 3, 5, 7, 12, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi 63-288055 JPO. Yamaguchi discloses (see, for example, figure 1) a first bipolar transistor (first semiconductor device) 50 and a second bipolar transistor (second semiconductor device) 40. The first bipolar transistor has a buried layer (first subcollector) 130 and the second bipolar transistor has a buried layer (second subcollector) 120. The buried layer in the first bipolar transistor 50 comprises arsenic and the buried layer in the second bipolar transistor 40 comprises antimony.

6. Claims 1, 5, 7 thru 9, 12, 20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Washio et al. 4,694,321. Washio discloses (see, for example, FIG. 2) a first bipolar transistor (first semiconductor device) 100 and an integrated injection logic (second semiconductor device) 200. The first bipolar transistor has a buried layer (first subcollector) 2 and the integrated injection logic has a buried layer (second subcollector) 22. In column 2, lines

35-40, Washio discloses the buried layer 22 having an impurity concentration greater than the buried layer 2.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khahezadeh 4,202,006. Khahezadeh does not disclose said first subcollector comprising an implant dose in the  $1 \times 10^{16} \text{ cm}^{-2}$  range and said second subcollector comprising an implant dose in the  $1 \times 10^{15} \text{ cm}^{-2}$  range. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use this range in order to have better emitter efficiency and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 6, Khahezadeh does not disclose said first subcollector having a sheet resistance below approximately 20 ohms/square, and said second subcollector having a sheet resistance above approximately 50 ohms/square said first subcollector having a sheet resistance below approximately 20 ohms/square, and said second subcollector having a sheet resistance above approximately 50 ohms/square. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have these sheet resistances, since it will

result in better emitter efficiency and higher inverse beta at relatively low breakdown and it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khajezadeh 4,202,006 as applied to claims 1-3, 5, 7-9, 12, and 21 above, and further in view of Hebert et al. 6,365,447 B1. Khajezadeh does not disclose said first subcollector comprising having an edge defined by a deep trench. However, Hebert discloses (see, for example, FIG. 2) a semiconductor wafer comprising buried layers 14, 16 and a vertical trench isolation structures. The trench isolation structures define the edges of the buried layers and separate adjacent devices. The trench isolations provide side wall isolation for adjacent devices. See, for example, column 5, lines 25-28. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the trench isolation structures of Hebert in Khajezadeh and have them define the edge of the subcollectors in order to provide side wall isolation between adjacent devices.

10. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi 63-288055 as applied to claims 1-3, 5, 7, 12, and 21 above, and further in view of Kamins et al. 5,633,179, and further in view of Chantre et al. 6,436,782 B2. Yamaguchi does not disclose the collector as being n-epi. However, Kamins teaches bipolar transistor wherein the collector is formed epitaxially. See, for example, the abstract wherein Kamins teaches a collector layer with an epitaxial structure. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to use the bipolar transistors' of Kamins (with the collector layer with an epitaxial structure) in Yamaguchi's invention in order to implement a different type of bipolar transistor (heterojunction bipolar transistor) well known in the art.

Yamaguchi in view of Kamins does not disclose a SiGe polysilicon p-doped extrinsic base and a Si Ge silicon single crystal intrinsic base. However, Chantre discloses a bipolar transistor comprising a SiGe layer (SiGe polysilicon p-doped extrinsic base) 3, and a p-doped base region of SiGe/Si layer (SiGe silicon single crystal intrinsic base) 2. It would have been obvious to one of ordinary skill in the art at the time of invention to include the SiGe layer and p-doped base region in Yamaguchi in view of Kamins in order to form an intrinsic and extrinsic base that reduces base resistance and, hence increases operation speed.

### ***Response to Arguments***

11. Applicant's arguments with respect to claims 1-10, 12-14, and 16-22 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the new limitation "to provide lateral ballasting of said second subcollector for providing ESD protection", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ 2d 1647 (1987). In addition, the claims and specification (see page 9, second paragraph) state that the limitation "to provide lateral ballasting of said second subcollector for providing ESD protection" is a product of the second subcollector differing from said first subcollector (i.e. first subcollector comprises an arsenic impurity and the second subcollector comprises an antimony

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impurity or dopant concentration differs between the subcollectors). Khajezadeh, Ohkawa, Yamaguchi, and Washio clearly disclose subcollectors of different impurity types or dopant concentrations as disclosed in the 102 rejections above.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

### **INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee  
October 5, 2003

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a large, sweeping initial 'E'.

**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**